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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,819	06/27/2003	Rajesh Kota	NWISP046	8385

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EXAMINER	
NASH, LASHANYA RENEE	
ART UNIT	PAPER NUMBER
2153	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,819	KOTA ET AL.	
	Examiner	Art Unit	
	LASHANYA R. NASH	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/11/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the request for continued examination 11 March 2008. Claims 1-31 are presented for further consideration. Claims 1, 12, and 23 are currently amended.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 March 2008 has been entered.

Response to Arguments

Applicant's arguments, See Remarks pages 7-10 with respect to claims 1, 12 and 23 have been fully considered and are persuasive in light of the amendments. Therefore, the rejection has been withdrawn. However, upon further consideration, new ground of rejection is made in view of newly found prior art, "Using Clustering for Effective Management of a Semantic Cache in Mobile Computing" and "Addressing the System-on-a-chip Interconnection Woes Through Communication-Based Design".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self et al. (US Patent 5,623,644) in view of Booth (US Patent 6,065,073) and Ren et al. "Using Clustering for Effective Management of a Semantic Cache in Mobile Computing" [retrieved from ACM] , hereinafter referred to as Self, Booth and Ren respectively.

In reference to claim 1, Self discloses a point-to-point communication apparatus (abstract). Self further discloses:

- A computer system (Figures 17-18), comprising:
- A first cluster (i.e. micro-cluster; Figure 18-item 1850; column 14, lines 1-14) including a first processor and a second processor of a plurality of processors (Figure 18-items 1812-1813) wherein the first processor is connected to the second processor through a point to point link (Figure 12a-processor 1201 and processor 1202 link to point-to-point interface 1205; column 10, lines 25-52), and the first processor is connected to the first interconnection controller (i.e. router/memory controller; Figure 18-

item 1811) through a point to point link (Figure 18-arrow from processor 1812 to router 1811) and the second processor is connected to the first interconnection controller through a point to point link (Figure 18-arrow from processor 1813 to router 1811), (i.e. point-to-point interconnection; column 14, lines 3-19);

- A second cluster (Figure 18-item 1851) including a second plurality of processors (Figure 18-processors for cluster 1851) and a second interconnection controller (Figure 18-router/memory controller), the second plurality of processors and the second interconnection controller in communication using a point-to-point architecture (column 10, lines 35-52; column 14, lines 10-26);

However, the reference fails to teach wherein disabling the second cluster comprises disabling polling for a link from the first interconnection controller to the second interconnection controller. Nonetheless, enabling and disabling polling was a well-known feature in the art, at the time of the invention, as further evidenced by Booth. Therefore, it would have been obvious for one of ordinary skill in the art to accordingly modify the features of Self.

In an analogous art, Booth discloses polling for network link (abstract). Booth further discloses wherein disabling the second cluster (i.e. interrupt signal is asserted; column 20, lines 43-45) comprises disabling polling for a link from the first interconnection controller to the second interconnection controller (column 19, line 45-50; column 20, line 55-column 21, line 6). One of ordinary skill in the art at the time of

the invention, would be motivated to according modify the system of Self with enabled/disabled polling so as to provide link monitoring for establishing communication links, while advantageously freeing up CPU bandwidth (i.e. disabling), (Booth; column 6, lines 30-40). However, the reference fails to disclose disabling the second cluster and emptying caches associated with the second cluster. Nonetheless, this would have been an obvious modification to the teachings of Self and Booth for one of ordinary skill in the art at the time of the invention, as further evidenced by Ren.

In an analogous art, Ren discloses a system for clustering of caches in a computing environment (abstract). Ren further discloses disabling a cluster and emptying the caches associated with the disabled cluster (i.e. cache removed from cluster and cache contents discarded/empty; page 96, lines 4-9). Thus, it would have been obvious for one of ordinary skill in the art to combine the known element of disabling a cluster and emptying cache, as taught by Ren, with the known element of disabling polling from a first interconnection controller to a second interconnection controller, as taught by Self and Booth, without substantial modification of their respective functions so as to yield the predictable result of disabling the second cluster and polling of the associated interconnection controller.

In reference to claim 2, Self shows the first cluster of processors and the second clusters of processors share a single virtual address space (column 11, lines 46-column 12, line 8).

In reference to claim 3, Booth shows wherein the first interconnection controller includes a physical layer enable indicator (column 13, lines 63-column 14, line 8).

In reference to claim 4, Self shows wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 14, lines 27-49).

In reference to claim 5, Self shows wherein the first interconnection controller includes a re-initialization indicator configurable to direct the first interconnection controller to reinitialize the link (column 8, lines 28-38; column 9, lines 15-27).

In reference to claim 6, Self shows wherein re-initialization comprises having a transmitter associated with the first interconnection controller send training sequence to the second interconnection controller (column 8, lines 28-38; column 9, lines 15-27).

In reference to claim 7, Booth shows wherein the transmitter sends the training sequence when the polling active state is set (column 20, line 55-column 21, line 6).

In reference to claim 8, Booth shows wherein the transmitter does not sent the training sequence when the polling sleep state is set (column 20, line 55-column 21, line 6).

In reference to claim 9, Self shows wherein re-initialization comprises having an associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 14, lines 10-26).

In reference to claim 10, Self shows wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 14, lines 11-26).

In reference to claim 11, Self shows wherein the first interconnection controller includes, fence, re-initialization and cluster ID bits (column 11, lines 46-column 12, line 8; column 11, lines 46-column 12, line 8) and Booth shows configuration space registers comprising physical layer enable (column 13, lines 63-column 14, line 8).

Claims 12-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self et al. (US Patent 5,623,644) in view Booth (US Patent 6,065,073) and Dervin et al (US Patent 6,952,766) and Sgroi et al. "Addressing the System-on-a-chip Interconnection Woes Through Communication-Based Design" [retrieved from ACM], hereinafter referred to as Self , Booth, Dervin and Sgroi respectively.

In reference to claim 12 and 23, Self discloses a point-to-point communication method and point-to-point apparatus communication (abstract), Self further discloses:

- A method for introducing a cluster of processors the method comprising:
    - Configuring a first interconnection controller (i.e. memory controller/router; Figure 18-item 1811) in a first cluster (Figure 18-item 1850) including a first plurality of processors (Figure 17-items 1711,1713; Figure 18-items

1812,1813) in communication using a point-to-point architecture (i.e. point-to-point interconnection; column 10, lines 35-52; column 14, lines 10-14);

- A second cluster (Figure 18-item1853) including a second plurality of processors (Figure 18-processors in 1853) in communication using a point-to-point architecture (i.e. point-to-point interconnection; column 14, lines 10-14).

However, the Self fails to disclose polling for the presence of a second interconnection controller. Nonetheless, enabling and disabling polling was a well-known feature in the art, at the time of the invention, as further evidenced by Booth. Therefore, it would have been obvious for one of ordinary skill in the art to accordingly modify the features of Self.

In an analogous art, Booth discloses polling for network link (abstract). Booth further discloses polling for a link to a second interconnection controller (column 20, line 55-column 21, line 6). One of ordinary skill in the art at the time of the invention, would be motivated to according modify the system of Self with enabled/disabled polling so as to provide link monitoring for establishing communication links, while advantageously freeing up CPU bandwidth (i.e. disabling), (Booth; column 6, lines 30-40). The references fail to show asserting a reset signal; and establishing, after asserting the signal, a link layer protocol on a connection between the first and second interconnection controllers. Nonetheless, this was a well-known feature in the art as disclosed by Dervin.

In an analogous art, Dervin discloses a method for automated node restart in clustered computing systems. Dervin further teaches asserting a reset signal (i.e. restart) and establishing, after asserting the signal, a link layer protocol on a connection (column 5, lines 34-48; column 7, lines 4-column 8, line 12; column 9, lines 7-18). One of ordinary skill in the art would have been so motivated to accordingly modify the method of Self, and Booth so as to automate the process of detecting and initiating the restart of polled clusters thereby increasing availability and reducing operator intervention (Dervin column 2, lines 58-62). However, the references fail to disclose enabling physical layer communications between the first and second interconnection controllers without enabling link layer communications between the first and second interconnection controllers, and after enabling the physical layer communication establishing a link layer protocol on a connection between the first and second interconnection controllers. Nonetheless, these features would have been obvious modifications to Self, Booth and Dervin for one of ordinary skill in the art at the time of the invention, as further evidenced by Sgroi.

In an analogous art, Sgroi discloses a communication based design of network-on-chip employing OSI layers model implementation (abstract). Sgroi further discloses enabling physical layer communications without enabling link layer communications (i.e. interface is actually the physical layer…no data-link layer is required; page 669, *An NOC Example:The Pleiades Platform*, paragraph 2) and after enabling the physical layer communication establishing a link layer protocol on a connection (page 670, *3.2. A Metropolis Example:Itercom*, paragraphs 3-5). One of ordinary skill in the art would have

been so motivated to accordingly modify the communications between the first and second interconnection controllers so as to implement protocols of the OSI layers that match the needs of the system components (i.e. not necessary to implement all of the OSI layers for high-functionality), (Sgori page 669, *2. OSI Reference Model Applied to NOCs*, paragraph 9).

In reference to claims 13 and 24, Booth discloses wherein polling is performed continuously (column 20, line 55-column 21, line 6).

In reference to claims 14 and 25, Booth shows wherein the first interconnection controller includes a physical layer enable indicator (column 13, lines 63-column 14, line 8).

In reference to claims 15 and 26, Self shows wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 14, lines 27-49).

In reference to claim s 16 and 27, Self shows wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link (column 8, lines 28-38; column 9, lines 15-27).

In reference to claims 17 and 28, Self shows wherein reinitialization comprises having a transmitter associated with the first interconnection controller send training sequence to the second interconnection controller (column 8, lines 28-38; column 9, lines 15-27).

In reference to claims 18 and 29, Booth shows wherein the transmitter sends the training sequence when the polling active state is set (column 20, line 55-column 21, line 6).

In reference to claims 19 and 30, Booth shows wherein the transmitter does not sent the training sequence when the polling sleep state is set (column 20, line 55-column 21, line 6).

In reference to claims 20 and 31, Self shows wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 14, lines 10-26).

In reference to claim 21, Self shows wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 14, lines 11-26).

In reference to claim 22, Self shows wherein the first interconnection controller includes, fence, reinitialization and cluster ID bits (column 11, lines 46-column 12, line 8; column 11, lines 46-column 12, line 8) and Booth shows configuration space registers comprising physical layer enable (column 13, lines 63-column 14, line 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaShanya R. Nash whose telephone number is (571)272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LaShanya R Nash/
Examiner, Art Unit 2153
March 28, 2008

/Glenton B. Burgess/
Supervisory Patent Examiner, Art Unit 2153